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(54) Coding for a multilevel transmission system

Kodierung für ein Vielfachpegel-Übertragungssystem

Codage pour un système de transmission à niveaux multiples

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Description

[0001] The present invention relates to an arrangement for communicating parameter values in a noisy environment.

[0002] Increasing the capacity and robustness to errors of communications and data storage systems have been the object of much research effort. In 'Weighted PCM' by Edward Bedrosian, IRE Transactions on Information Theory, March 1958 a technique is described in which the relative amplitudes of the pulses in a pulse code modulation scheme are adjusted to minimise the noise power of the reconstructed signal due to errors in transmission. In brief, those pulses which have a greater effect on the reconstructed signal are transmitted at a higher amplitude than the others, subject to the constraint that the overall message power transmitted is constant. A performance analysis described in the paper exhibits a significant increase in signal to noise ratio. Such techniques, however, have not been widely used and it has been suggested that this is due to the higher power capability and large number of different quantisation levels required at the transmitter. In addition there has been an increase in emphasis on modulation schemes and error correction coding.

[0003] EP-A-0 490 552 discloses a system for applying unequal error protection to a high definition TV (HDTV) signal. More particularly the system comprises means for dividing the HDTV signal into a plurality of classes of information, separately coding each one of the plurality of classes of information using different coded modulation schemes and multiplexing the plurality of coded outputs for transmission. Each of the coded outputs comprises the sum of the number of bits applied to the modulator plus the number of redundant bits introduced by the encoder. Thus the multiplexer output has a larger overall number of bits compared to those in the original HDTV signal.

[0004] EP-A-0 282 298 discloses a method for combining encoding and modulation of digital information for transmission through an information channel. The method comprises indexing digital signals representative of elementary modulations by indexing vectors to create a decomposition of indexing vectors of an index vector space into a plurality of ordered subspaces, including binary and nonbinary subspaces; associating with each said indexing vector a Euclidean distance in modulation space such that any two modulations whose indexing vectors differ only by a distance vector contained in a first subspace and any preceding (higher significant) subspaces of the series of ordered subspaces are separated in said modulation space by at least said Euclidean distance; and encoding information signals by encoders employing error-correcting codes, each said encoder producing a symbol representative of an indexing vector of the same dimension as a corresponding one of said ordered subspaces for communication of said symbol through said information channel.

[0005] It is an object of the present invention to minimise noise in parameter values which are transmitted to a receiver or stored for later recall.

[0006] According to a first aspect of the present invention there is provided an arrangement for coding a continuous stream of parameter values consisting of a plurality of bits, characterised by means for separating the plurality of bits into at least two sections according to whether they are more or less significant, first means for encoding more robustly a bit in the more significant section as a separate symbol, second means for encoding at least 2 bits in the less significant section as a single symbol, means for combining said symbols produced by said first and second means to produce an output signal in which the duration of the total number of symbols does not exceed the duration of the total number of symbols represented by encoding each bit as a respective symbol.

[0007] The present invention also provides an arrangement for transmitting a continuous stream of parameter values, comprising the arrangement as claimed in Claim 1 together with the additional feature of means for transmitting said output signals.

[0008] The present invention further provides an arrangement for communicating a continuous stream of parameter values, comprising the arrangement as claimed in Claim 1 together with the additional features of means for recovering said output signal, means for separating symbols representative of bits in the more significant section from the remaining symbols in said recovered signal, means for decoding said bits represented by said symbols and means for supplying a plurality of bits in the correct order of significance.

[0009] By generating at least two symbols based upon a digital data word, the more significant bit or bits of the word can be transmitted in a reliable manner using for example bi-level (binary) amplitude modulation or other robust signalling. The less significant bits are considered as one or more sub-sections each representing a larger number of states and these are converted to one or more multi-state symbols for transmission in a shorter time interval than would apply if binary modulation were used. The less significant bits are more prone to error using such a technique but the gain in channel capacity outweighs this disadvantage where parameters or quantised analogue quantities are being transmitted. This gain in channel capacity may be used to improve the channel robustness or to provide extra channels.

[0010] The less significant bits may thus be transmitted using, for example, amplitude modulation, quadrature amplitude modulation (QAM), quadrature phase shift keying (QPSK) or 8-PSK while the more significant bits are transmitted using bi-level or bi-phase modulation, 3-level modulation and so on. Longer words may be separated into a greater number of sub-sections, for example an eight bit digital word may be encoded as four 2-state symbols, a 3-state symbol and an 8-state symbol. A word which is coded in accordance with the present invention may comprise a non-integer

number of bits. The boundaries between bits in the word will not necessarily correspond to the boundaries between symbols.

[0011] The length of time for which a symbol is transmitted also directly affects the likelihood of error. The time saved, compared to a purely bi-level system, by representing the less significant bits of a data word as a multilevel signal having 3 or more levels could be used to increase the duration of the symbol or symbols representing the most significant bit or bits. The duration of such a symbol may conveniently be an integer multiple of the duration of the other symbols used to represent a word but other durations are possible.

[0012] Two symbols may be transmitted simultaneously in different modulation dimensions using, for example, Quadrature Amplitude Modulation or Phase Shift Keying.

[0013] Providing the most robust transmission for the most significant bits of a data word is particularly applicable to a system for communicating digitised analogue signals. For such a purpose, means are provided to digitise the analogue signals at the input to the system and to derive a replica of the digitised signals at the output of the system.

[0014] A four-bit data word may, by use of the present invention, be represented by two 2-state symbols for the two most significant bits and one 4-state symbol for the two least significant bits. The saving in time thus effected may be used to double the length of the symbol representing the most significant bit with a consequent reduction in its susceptibility to error.

[0015] An eight-bit data word may be represented by four 2-state symbols for the four most significant bits and by two further symbols for the remaining bits. For example, the four least significant bits could be represented by two 4-state symbols or by a 3-state symbol and an 8-state symbol. The latter option may be arranged to leave two of the possible states of the 8-state symbol unused which may be used to provide a useful extra clearance between certain adjacent states.

[0016] The allocation of transmission time to particular bits within a word may be made in non-integer subdivision of a clock interval. This may, however, have an effect on successful clock recovery at a receiver.

[0017] The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block schematic diagram of a data transmission arrangement in accordance with the present invention,

Figure 2 is a block schematic diagram of a data reception arrangement for use with the transmission arrangement of Figure 1,

Figure 3 shows the possible output levels when the transmission arrangement of Figure 1 is used to encode a four bit data word,

Figure 4 is a graph of a comparison of error probability between a standard binary signalling system and an arrangement which uses a four-level symbol,

Figure 5 is a graph of the effect of using a four-level symbol in a multilevel symbol technique on communicated signal to noise ratio at varying channel signal to noise ratios,

Figure 6 is a block schematic diagram of a transmission arrangement in accordance with the invention for transmitting 8-bit data words,

Figure 7 is a block schematic diagram of a reception arrangement for use with the transmission arrangement of Figure 6,

Figure 8 shows the possible output levels of the transmission arrangement of Figure 6,

Figure 9 is a graph of a comparison of error probability between a standard bi-level signalling system and the arrangements of Figures 6 and 7,

Figure 10 is a graph of error probability for a bi-level system and two multilevel techniques coding a 4-bit word using non-integer clock interval multiples, and

Figure 11 is a graph of error probability for a standard bi-level signalling system and a multilevel technique coding an eight-bit word using non-integer clock interval multiples.

[0018] In Figure 1 a four bit digital data word is fed to an input 10 to a splitting device 12 which separates the word into the two most significant bits and the two least significant bits. If the four bit digital word is supplied in a parallel format, the splitting device 12 may be no more elaborate than tracks printed on a circuit board. Where the word is supplied in a serial format the device 12 may comprise a multiplexer. The two most significant bits are fed to a bi-level modulation device 14 which is arranged to provide a signal having a first level if the binary signal is a 'one' and a second level if the binary signal is a 'zero'. Typically these levels will be assigned the arbitrary values of plus one and minus one respectively. The device 14 provides a pair of symbols each of which represents one of the two most significant bits of the data word in a bi-level format and having a length of one clock interval. The two least significant bits are fed to a four-level modulation device 16 which provides an output symbol one clock interval long which represents the two bits as a single symbol which may assume any one of four states. Multilevel modulation is described in greater detail in 'Digital Trans-

mission Systems' by David R. Smith, published by Van Nostrand Reinhold. The modulated symbols are fed to a combining device 18 which places them in an appropriate order for transmission and provides them to a transmitter (Tx) 20 for transmission over a channel. While a transmitter for a radio system is depicted, transmission may be effected over alternative channels, for example a fixed line or an optical fibre link, or the symbols may be stored in an appropriate medium, for example magnetic or optical, for later retrieval.

[0019] Figure 3 shows the possible states of the output of the combining device 18 of Figure 1 during a first clock interval b1, a second clock interval b2 and a third clock interval b3. It is apparent from the drawing that the four-level signal which occupies clock interval b3 has a higher peak amplitude than the two-level signals in the first and second clock intervals. This is so that the symbol transmitted in the third clock interval has the same average power as each of those transmitted in the first two. If it is assumed that the peak amplitude of the multi-level symbol is a, that the levels are equidistant and all equally likely, then $\frac{1}{2}(a^2 + (1/3\ a)^2) = 1$ which gives a = 1.34.

[0020] A more general formula for a is

$$a = \sqrt{3\frac{S-1}{S+1}}$$

where S is the number of states which the symbol may assume. Where the likelihood of occurrence of particular states differs, the average expected power is the sum of the powers of the levels multiplied by their probability of occurrence.

[0021] Figure 2 shows a reception arrangement for use with the arrangement of Figure 1 in which a receiver (Rx) 22 has an output which is coupled to a splitting device 24 having two outputs. A first output is coupled to a demodulator 26 and a second output is coupled to a demodulator 28. The bi-level symbols are demodulated in the demodulator 26 to provide a binary output to a first input of a combining device 30. The four-level symbol is demodulated in the demodulator 28 to provide a binary output to a second input of the combining device 30. The combining device 30 provides a four bit word at an output bus 32. The device 30 may be no more complex than tracks on a printed circuit board if the outputs of the demodulators are in parallel and are active simultaneously.

[0022] Figure 4 shows the error performance of a four level symbol when compared to a pair of bi-level symbols using a root mean square (RMS) error criterion. The horizontal axis S/N is the signal to noise ratio of the channel over which communication is to occur expressed in dB and the vertical axis is the probability of error P expressed in negative powers of ten. The dashed lines 1q, 2q and 3q represent the probabilities of an error of distance 1, (in other words, 1 sent, 2 received, 4 sent, 3 received and so on) distance 2 and distance 3 respectively, using a single four-level symbol. The probability of an error of distance 1 is quite likely but errors of distance 2 or 3 are rather unlikely. The solid lines 1b, 2b and 3b represent the probabilities of an error distance of either 1 or 2 and an error of distance 3, respectively, when using two, 2-level symbols. The probabilities of an error distance of 1 or 2 are virtually equal since these correspond to a single error in the less significant bit and to a single error in the more significant bit respectively. The error probabilities are not quite the same because of the small but finite chance of having an error in both bits, which marginally increases the probability of an error distance of one as a result of the possibility of the corruption from 10b to 01b and vice versa. As can be observed, the likelihood of an error of distance 1 using the two, 2-level symbols is much less likely than when using a single 4-level signal. However, the likelihood of error of distance 2 using the two, 2-level symbols is significantly more likely than when using a 4-level symbol. Where parameters or continuously varying quantities are being transmitted in a digital format, an error in the least significant bit may well go unnoticed but errors in more significant bits may well be intolerable. In such circumstances the performance of the 4-level symbol could well be preferable to that of the two, 2-level symbols.

[0023] Figure 5 shows the communicated (COM) signal to noise (S/N) ratio on the vertical axis against channel (CH) signal to noise ratio on the horizontal axis for a four-bit data word transmitted in four clock intervals as four 2-level symbols (B) and in three clock intervals as two 2-level symbols and a 4-level symbol (M1). At channel S/N ratios of 7 dB or less the communicated S/N ratios are virtually identical but above 7 dB the pure 2-level system has superior performance. Also plotted in the Figure as a broken line is the magnitude of the least significant bit, 6dB x 4 = 24dB. It can be argued that accuracy much greater than that of the least significant value bit is of no practical use when communicating parameter values. Indeed, there will often not have been any greater accuracy in the source signal, which may have been quantised to 4 bits and subject to quantisation noise accordingly. A recovered rms error value that is significantly less than the smallest bit is therefore of little advantage and if it can be traded for another property then it should be. In the case of the multilevel technique here, it has been traded for a reduction in transmission time.

[0024] Figure 5 also shows a curve (M2) which is the communicated S/N ratio against channel S/N ratio for a four-bit data word transmitted as three 2-level symbols and a 4-level symbol, the most significant bit being transmitted as two, 2-level symbols. The performance using this technique is better than that of the three symbol technique at channel S/N ratios of less than approximately 11 dB and better than the four 2-level symbol technique at channel S/N ratios of less than approximately 9 dB. Both of the techniques which use a 4-level symbol are limited in their performance by the pres-

ence of that symbol when a good channel is available.

[0025] Two symbols may be transmitted simultaneously in different modulation dimensions using quadrature channels for example. Consider a three bit word encoded as a 2-level symbol for the most significant bit and a 4-level symbol for the remaining bits. Instead of transmitting the two symbols during different clock intervals, a first quadrature channel can transmit the 2-level symbol and a second quadrature channel can transmit the 4-level symbol. Because of the greater peak amplitude of the 4-level symbol as described previously, the peak amplitude of the signal in the second quadrature channel is greater than that of the first quadrature channel. Thus the two symbols are combined in different modulation dimensions rather than in different clock intervals. Alternatively this symbol combination may be considered as a quadrature amplitude modulated (QAM) signal in which one of the modulation dimensions is weighted differently to the other.

[0026] Using the previous 4 symbol example, one quadrature channel could carry two 2-level symbols representing the most significant bit one symbol after the other while at the same time the other channel could carry the remaining 2-level symbol followed by the 4-level symbol. This is analogous to a QAM arrangement comprising a clock interval containing 4-QAM signal and a clock interval containing an 8-QAM signal with differently weighted modulation dimensions.

[0027] The two symbols representing different respective numbers of states in accordance with the invention may comprise a traditional QAM symbol (having equal interstate separations in the two dimensions) together with a one dimensional multi-level symbol or even a QAM symbol representing fewer states. QAM is described in more detail in the book 'Digital Transmission Systems' identified above. Briefly, in 16-QAM four different levels in each of two different modulation dimensions combine to provide 16 separate states. This modulation may be used for less significant bits of a word while 2-level (or 3-level and so on) modulation is used for the more significant bits. One possible allocation for the values of a digital word applied to a 16-QAM signal is shown as a simple grid, thus:

1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16

[0028] The aim when assigning states to the word values is to arrange for the values of adjacent states of the modulation to provide the minimum RMS error on reception or decoding when adjacent states are mistaken for one another, for example due to noise on a communication channel.

[0029] A 16-QAM signal may be used to represent sixteen states which correspond to four bits of a digital word and so enable longer digital words to be communicated in fewer clock intervals. Alternatively such a signal could be used, for example, to represent ten or twelve different states and error detection or correction coding which is known in the art could be applied to these states to exploit the remaining available states in 16-QAM.

[0030] As a further alternative the 16-QAM symbol may be used to represent fewer than sixteen states without attempting to use all or any of the unused states to provide error coding. The greater distance between certain adjacent states will provide an improvement in performance in its own right. For example, the allocation of 14 of the 16 states as depicted below results in approximately 75% of the RMS error of the allocation of 16 states shown above:

1	2	4	7
3	5		9
6		10	12
8	11	13	14

[0031] Fewer still of the states could be allocated to provide more robust transmission. A coding system in accordance with the invention may thus provide a plurality of 16-QAM signals to encode a word. The more significant bits of the word will be encoded with a less-dense (or sparse) 16-QAM allocation than the less significant bits. Such less-dense QAM allocations can conveniently be considered as one symbol rather than as two symbols in different modulation dimensions since the QAM signal cannot readily be decomposed into symbols representing different numbers of states. Where the smallest interstate separation in the two dimensions differs, this can be considered as two symbols in differ-

ent modulation dimensions even if not every state in those two symbols is allocated.

[0032] The exploitation of multi-dimensional modulation in accordance with the invention may be extended to three dimensions and beyond.

[0033] Figure 6 shows a transmission arrangement in accordance with the present invention for transmitting digitally encoded analogue signals. A source of analogue signals, depicted as a microphone 34 has an output coupled to a code excited linear prediction (CELP) analogue signal coding arrangement 36. Other types of coding arrangement are suitable for use in the transmission arrangement, particularly parameter-based arrangements such as vocoders. The output of the arrangement 36 is a set of digital parameter values comprising up to eight bits each and these are supplied in sequence to a splitting device 38 having three outputs. A first output of the device 38 comprises the four most significant bits of the parameters and this output is fed to a bi-level modulation device 40 which provides four 2-level modulated symbols to a first input of a combining device 46. A second output of the device 38 comprises the fifth and sixth most significant bits of the parameter and is fed to a first multilevel modulation device 42. An output of the device 42 is a three-level symbol which is fed to a second input of the combining device 46. A third output of the device 38 comprises the sixth, seventh and eighth most significant bits of the parameter and is fed to a second multilevel modulation device 44. An output of the device 44 is an 8-level symbol which is fed to a third input of the combining device 46. The device 46 arranges the six symbols into a serial stream and couples them to a transmitter (Tx) 48 for transmission. In this arrangement the four least significant bits, which may represent one of sixteen states are sub-divided into a factor of three represented by a three-level symbol and the factor of six represented by an eight-level symbol. A six-level symbol could be used in place of the eight level symbol. Alternatively, error detection or correction coding could be applied to the least significant bits to provide twenty-four states altogether, thus fully exploiting the states which may be represented by the three-level and the eight-level symbols. More simply the states of the digital word could be applied to the eight-level symbol to maximise the distance of the states from each other and provide more robust coding as described above. Of course certain parameters produced by the arrangements 36 may have no particular weighting towards any of the bits which they comprise and these parameters may be transmitted using a purely 2-level technique or the same multilevel symbols for the whole parameter in the usual manner. The splitting device 38 may thus be arranged to apply the whole of such a parameter to the appropriate modulation device.

[0034] Figure 8 shows the possible states of the output of the combining device 46 (Figure 6) during clock intervals b1 to b6. The 3-level symbol in interval b5 has the effect of decreasing the significance of the following symbol, reducing the level of its error contribution.

[0035] Figure 7 shows a reception arrangement for use with the transmission arrangement of Figure 6. A radio receiver (Rx) 50 has an output which is coupled to a splitting device 52 having three outputs. A first output of the device 52 is fed to a bi-level demodulator 54 and comprises the four 2-level symbols of the received signal. A second output of the device 52 is fed to a 3-level demodulator 56 and comprises the 3-level symbol of the received signal. A third output of the device 52 is fed to an 8-level demodulator 58 and comprises the 8-level symbol of the received signal. Outputs of the three demodulators are fed to respective inputs of a combining device 60 which converts the demodulated signals to a parallel data word. The parallel data word is fed to a CELP analogue signal re-synthesising device 62 whose output is coupled to a transducer, in this case a loudspeaker 64.

[0036] The arrangements of Figures 6 and 7 are applicable to the communication of signals other than analogue signals if the analogue signal encoding and decoding devices are omitted. An eight bit word may thus be transmitted in just six clock intervals. Longer words may also be communicated by selecting appropriate symbols and using more clock intervals.

[0037] Figure 9 shows a graph comparing the performance of the transmission arrangement of Figures 6 and 7 with a system in which all eight bits are encoded as bi-level symbols. The vertical axis (COM) is the communicated S/N ratio of the transmitted signals and the horizontal axis (CH) is the channel S/N ratio. The curve B shows the performance of the bi-level system in 8 clock intervals and the curve M shows the performance of the multilevel technique in 6 clock intervals. As can be seen the performance of the two systems are virtually identical for channel S/N ratios below 11 dB and do not differ to a great extent even at S/N ratios greater than this. As in Figure 5 a broken line is included in the Figure to indicate the limit of useful accuracy, in this case 48dB. As can be seen the multilevel technique produces virtually the same performance up to this limit.

[0038] As an alternative to amplitude modulation, multi-state symbols may be generated by Phase Shift Keying (PSK) where the particular states are modulated at the transmitter as a series of phase or angle variations. Binary PSK is capable of sending one of two possible states per symbol by using one of two signals at relative phase shifts of 0 and π respectively. Quadrature PSK uses relative phase shifts of 0, $\pi/2$, π and $3\pi/2$ radian and 8-PSK uses relative phase shifts of 0, $\pi/4$, $\pi/2$, $3\pi/4$, π, $5\pi/4$, $3\pi/2$ and $7\pi/4$ radian.

[0039] A system in accordance with the invention which uses PSK may comprise the arrangement of Figure 1 in which the modulation devices 14,16 are arranged to provide two binary PSK symbols and a quadrature PSK symbol respectively. The combining device 18 and the Tx 20 are arranged to operate with PSK signals. Similarly the Rx 22, splitting device 24 and demodulation devices 26,28 of Figure 2 are arranged to operate with PSK signals. The use of PSK may

be extended to further multistate symbols such as a combination of binary, quadrature and 8-PSK in a similar manner to that described for multi-level symbols above.

[0040] On reception of PSK signals, when an error is made a signal sent as one state is equally confusable with the two adjacent states as is the case for amplitude modulation. However, there is an additional complication due to the nature of PSK, that of a cyclic error effect, meaning that a phase signal transmitted as 0 radian in 8-PSK may be received as $\pi/4$ radian or $7\pi/4$ radian with equal probability. Thus, if a straightforward allocation were to be made of the eight states represented by the digital word to those of the PSK, there could be an error in transmission of a single phase graduation which would cause a signal transmitted in the first state to be received as a signal in the last state and vice versa. To prevent such a minor error of just one phase graduation from affecting the received value to such an extent the eight states of the word could be allocated to PSK phases as follows:

State	Phase
1	0 rad
3	$\pi/4$
5	$\pi/2$
7	$3\pi/4$
8	π
6	$5\pi/4$
4	$3\pi/2$
2	$7\pi/4$

[0041] Thus a transmission error of one phase graduation, or $\pi/4$, can never result in a perceived error in a digital word having a magnitude of more than two states.

[0042] Different styles of state allocation may be applied to PSK coding using different numbers of states. For example, where a 12-state symbol is used a straightforward allocation would be:

1 2 3 4 5 6 7 8 9 10 11 12

but the RMS error may be reduced by 4dB using the following allocation:

1 2 3 5 6 8 9 11 12 10 7 4.

A further slight improvement can be obtained using:

1 3 5 7 9 11 12 10 8 6 4 2.

[0043] In a similar manner to the above combination of two multi-state symbols in different modulation dimensions, two symbols can be combined in a single PSK signal. For example a 2-state symbol and a 4-state symbol could be combined by allocating 0 radian to one of the states of the 2-state symbol and π radian to the other state. The states of the 4-state symbol could be allocated $-\pi/4$, $-\pi/12$, $+\pi/12$ or $+\pi/4$ respectively. A combination of the two symbols results in an eight state symbol with unequal interstate graduations. There is a minimum angle of $\pi/2$ between the states of the 2-state symbol and a minimum angle of $\pi/6$ between the states of the 4-state signal, thus providing different degrees of protection to the most significant bit and the remaining bits.

[0044] As was observed earlier, with reference to Figure 5, representing the most significant bit by more than one symbol has quite a noticeable effect on the performance of the system when compared with a most significant bit communicated in just one clock interval. This effect can be extended to alteration of the duration of all of the symbols to be transmitted.

[0045] In the case of the four-bit word, the saving of one clock interval by using multiple symbol signalling as opposed to a pure 2-level system, can be used to extend the duration of the three symbols by a factor a 4/3. The channel noise will be reduced by 10 log [4/3] = 1.25 dB with a consequent improvement in the sensitivity of the communication system. However there may be problems with clock recovery at the receiving end of the system.

[0046] Alternatively the duration of the symbols can be made different from each other. One possible allocation of 4 clock intervals to a four-bit word is:

Message bit	Symbol	Symbol Duration
1 (MSB)	bi-level	2.25
2	bi-level	1.25
3	4-level	0.5
4		

[0047] To transmit a four-bit word in three clock intervals, a possible allocation is:

Message bit	Symbol	Symbol Duration
1 (MSB)	bi-level	1.6
2	bi-level	0.9
3	4-level	0.5
4		

[0048] Figure 10 shows the communicated S/N ratio (COM) on the vertical axis against the channel S/N ratio (CH) on the horizontal axis for a pure bi-level symbol scheme (B), the four clock interval (M1) scheme and three clock interval (M2) scheme above. By comparison with Figure 5 the improvement in performance of the non-integer clock interval allocations over a system in which the symbol edges coincide with the clock interval boundaries can be seen. The four clock interval scheme has a sensitivity of 1.7 dB better than the pure bi-level scheme while even the three clock interval scheme can out-perform the pure bi-level system, despite occupying only three quarters of the transmission time. As before, a limit of useful accuracy is shown by a broken line at 24dB communicated S/N.

[0049] Unequal symbol durations can be applied to a system for encoding an 8-bit data word in 8 clock intervals. One possible allocation is as follows:

Message bit	Symbol	Symbol Duration
1 (MSB)	bi-level	1.78
2	bi-level	1.47
3	bi-level	1.21
4	bi-level	0.95
5	3-level	1.64
6		
7	8-level	0.95
8		

[0050] Figure 11 shows a graph of communicated S/N ratio (COM) on the vertical axis against channel S/N ratio (CH) on the horizontal axis for the pure 2-level symbol scheme (B) and the multiple-level symbol scheme (M). The pure 2-level scheme can be seen to provide inferior performance to the multiple-level symbol scheme M at channel S/N ratios below approximately 12.5 dB. In very poor channels the error values are maintained using the multiple-level symbol scheme with channel S/N ratios of up to 2 dB worse than the pure 2-level scheme. As previously, the limit of useful accuracy, 48dB, is shown in a broken line.

[0051] As an alternative to non-coincident symbol durations and clock intervals, the communication time saved by the invention may be used to apply error correction or detection codes to the more significant bits of the digital word. One suitable code would be a convolutional code which provides two output bits for each input bit. Other coding techniques, such as Hamming Codes may be applied. Error detection or correction coding bits for those more significant bits, which are probably communicated as two-state symbols, may be arranged to be communicated with the less significant bits as part of a multi-state symbol.

[0052] From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of systems for communicating digital data words and component parts thereof and which may be used instead of or in addition to features already described herein.

Claims

1. An arrangement for coding a continuous stream of parameter values consisting of a plurality of bits, characterised by means (12,36) for separating the plurality of bits into at least two sections according to whether they are more or less significant, first means (14,40) for encoding more robustly a bit in the more significant section as a separate symbol, second means (16,44) for encoding at least 2 bits in the less significant section as a single symbol, means (18,46) for combining said symbols produced by said first and second means to produce an output signal in which the duration of the total number of symbols does not exceed the duration of the total number of symbols represented by encoding each bit as a respective symbol.

2. An arrangement as claimed in claim 1, characterised in that said second means (16,44) encodes a plurality of bits as a single multi-level symbol.

3. An arrangement as claimed in claims 1 or 2, characterised in that the first and second means (14,16,40,44) produce symbols having a substantially equal average power.

4. An arrangement as claimed in any one of claims 1 to 3, characterised in that each symbol is of substantially equal duration.

5. An arrangement as claimed in any one of claims 1 to 3, characterised in that the first means (14,40) encodes the most significant bit as two symbols.

6. An arrangement as claimed in any one of claims 1 to 3, characterised in that the symbols produced by said first means (14,40) are of a longer duration than the symbols produced by said second means (16,44).

7. An arrangement for transmitting a continuous stream of parameter values consisting of a plurality of bits, comprising an arrangement as claimed in any one of claims 1 to 6 and means (20,48) for transmitting said output signal.

8. An arrangement as claimed in claim 7, characterised in that the transmitting means (20, 48) comprises a phase shift keying transmitting means for transmitting at least one symbol from said first means (14,40) simultaneously with at least one symbol from said second means (16,44).

9. An arrangement for communicating a continuous stream of parameter values consisting of a plurality of bits, comprising an arrangement as claimed in any one of claims 1 to 6, means(22,50) for recovering said output signal, means for separating symbols representative of bits in the more significant section from the remaining symbols in said recovered signal, means (26,28,54,58) for decoding said bits represented by said symbols and means (30,60) for supplying a plurality of bits in the correct order of significance.

10. An arrangement as claimed in Claim 9, characterised in that the combining means (18,46) comprises transmitting means for transmitting at least one symbol from said first means (14,40) simultaneously with at least one symbol from said second means (16,44).

Patentansprüche

1. Anordnung zur Codierung eines kontinuierlichen Stroms von Parameterwerten, die aus einer Vielzahl von Bits bestehen, dadurch gekennzeichnet, dass sie folgendes enthält: Mittel (12, 36) zum Aufteilen der Vielzahl von Bits in mindestens zwei Abschnitte, je nachdem, ob sie eine höhere oder eine geringere Wertigkeit aufweisen; erste Mittel (14, 40) zum zuverlässigeren Codieren eines Bits in dem Abschnitt mit höherer Wertigkeit als ein getrenntes Symbol; zweite Mitte (16, 44) zum Codieren von mindestens 2 Bits in dem Abschnitt mit geringerer Wertigkeit als ein einziges Symbol; Mittel (18, 46) zum Kombinieren der durch die genannten ersten und zweiten Mittel erzeugten Symbole, um ein Ausgangssignal zu erzeugen, wobei die Dauer der Gesamtzahl der Symbole nicht die Dauer der Symbole überschreitet, die durch Codieren jedes Bits als ein entsprechendes Symbol dargestellt werden.

2. Anordnung nach Anspruch 1, dadurch gekennzeichnet, dass die genannten zweiten Mittel (16, 44) eine Vielzahl von Bits als ein einziges Vielfachpegelsymbol codieren.

3. Anordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, dass die ersten und zweiten Mittel (14, 16, 40, 44) Symbole mit einer im wesentlichen gleichen Durchschnittsleistung erzeugen.

4. Anordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass jedes Symbol im wesentlichen die gleiche Dauer hat.

5. Anordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass die ersten Mittel (14, 40) das Bit mit der höchsten Wertigkeit als zwei Symbole codieren.

6. Anordnung nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, dass die von den genannten ersten Mitteln (14, 40) erzeugten Symbole eine längere Dauer als die von den genannten zweiten Mitteln (16, 44) erzeugten Symbole haben.

7. Anordnung zum Übertragen eines kontinuierlichen Stroms von aus einer Vielzahl von Bits bestehenden Parameterwerten, die eine Anordnung nach einem der Ansprüche 1 bis 6 und Mittel (20, 48) zum Übertragen des genannten Ausgangssignals enthält.

8. Anordnung nach Anspruch 7, dadurch gekennzeichnet, dass die Übertragungsmittel (20, 48) Übertragungsmittel mit Phasenumtastung enthalten, um mindestens ein Symbol von den genannten ersten Mitteln (14, 40) gleichzeitig mit mindestens einem Symbol von den genannten zweiten Mitteln (16, 44) zu übertragen.

9. Anordnung zum Übertragen eines kontinuierlichen Stroms von aus einer Vielzahl von Bits bestehenden Parameterwerten, die folgendes beinhaltet: eine Anordnung nach einem der Ansprüche 1 bis 6, Mittel (22, 50) zum Wiederherstellen des genannten Ausgangssignals, Mittel zum Trennen der Bits in dem Abschnitt mit höherer Wertigkeit darstellenden Symbole von den übrigen Symbolen in dem genannten wiederhergestellten Signal, Mittel (26, 28, 54, 58) zum Decodieren der genannten durch die genannten Symbole dargestellten Bits und Mittel (30, 60) zum Liefern einer Vielzahl von Bits in der richtigen Reihenfolge der Wertigkeit.

10. Anordnung nach Anspruch 9, dadurch gekennzeichnet, dass die Kombinationsmittel (18, 46) Übertragungsmittel zum gleichzeitigen Übertragen von mindestens einem Symbol von den genannten ersten Mitteln (14, 40) gleichzeitig mit mindestens einem Symbol von den genannten zweiten Mitteln (16, 44) enthalten.

Revendications

1. Montage pour codage d'un train continu de valeurs paramétriques constitué d'une pluralité de bits, caractérisé par un moyen (12,36) pour séparer la pluralité de bits en au moins deux sections selon qu'ils soient plus ou moins significatifs, un premier moyen (14,40) servant à coder plus solidement un bit dans la section la plus significative sous forme de symbole séparé, un deuxième moyen (16,44) servant à coder au moins deux bits dans la section la moins significative en un symbole unique, un moyen (18,46) pour combiner lesdits symboles produits par ledit premier et ledit deuxième moyens pour produire un signal de sortie dans lequel la durée du nombre total de symboles ne dépasse pas la durée du nombre total de symboles représentés en codant chaque bit sous la forme d'un symbole respectif.

2. Montage selon la revendication 1, caractérisé en ce que ledit deuxième moyen (16,44) code une pluralité de bits sous la forme d'un symbole unique à niveaux multiples.

3. Montage selon les revendications 1 ou 2, caractérisé en ce que le premier et le deuxième moyens (14,16,40,44) produisent des symboles ayant une puissance moyenne sensiblement égale.

4. Montage selon l'une quelconque des revendications 1 à 3, caractérisé en ce que chaque symbole est de durée sensiblement égale.

5. Montage selon l'une quelconque des revendications 1 à 3, caractérisé en ce que le premier moyen (14,40) code le bit le plus significatif sous la forme de deux symboles.

6. Montage selon l'une quelconque des revendications 1 à 3, caractérisé en ce que les symboles produits par ledit premier moyen (14,40) ont une durée plus longue que les symboles produits par ledit deuxième moyen (16,44).

7. Montage pour la transmission d'un train continu de valeurs paramétriques comprenant une pluralité de bits, comprenant un montage selon l'une quelconque des revendications 1 à 6 et un moyen (20,48) pour transmettre ledit signal de sortie.

8. Montage selon la revendication 7, caractérisé en ce que le moyen de transmission (20,48) comprend un moyen de transmission à modulation par déplacement de phase pour transmettre au moins un symbole dudit premier moyen (14,40) simultanément avec au moins un symbole dudit deuxième moyen (16,44).

9. Montage pour transmettre un train continu de valeurs paramétriques comportant une pluralité de bits, comprenant un montage selon l'une quelconque des revendications 1 à 6, un moyen (22,50) pour récupérer ledit signal de sortie, un moyen pour séparer des symboles représentatifs de bits de la section la plus significative des symboles restant dans ledit signal récupéré, un moyen (26,28,54,58) pour décoder lesdits bits représentés par lesdits symboles et un moyen (30,60) pour délivrer une pluralité de bits dans l'ordre correct de signification.

10. Montage selon la revendication 9, caractérisé en ce que le moyen de combinaison (18,46) comprend un moyen de transmission pour transmettre au moins un symbole dudit premier moyen (14,40) simultanément avec au moins un symbole dudit deuxième moyen (16,44).

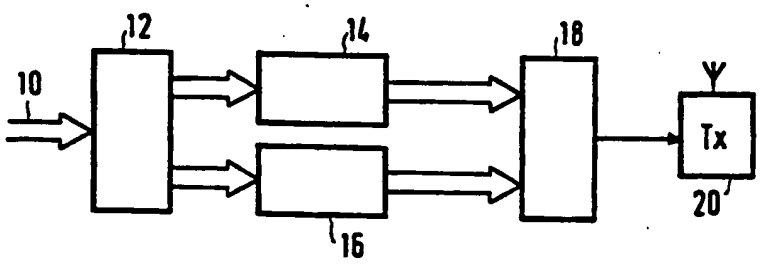

FIG.1

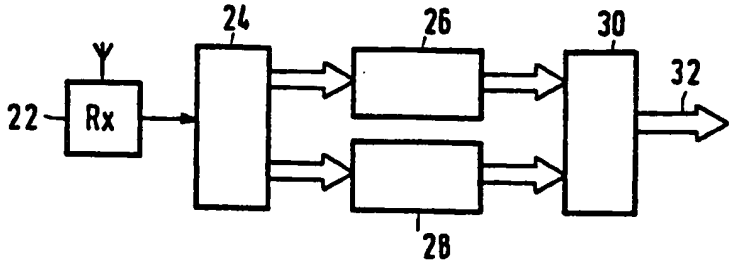

FIG.2

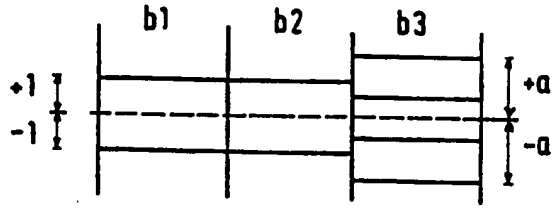

FIG.3

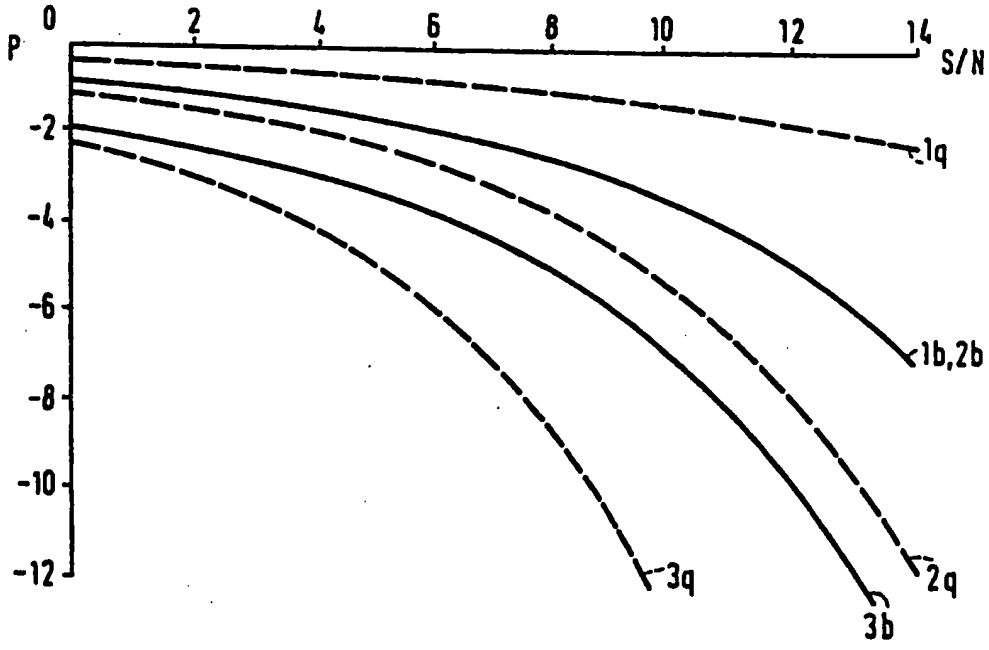

FIG.4

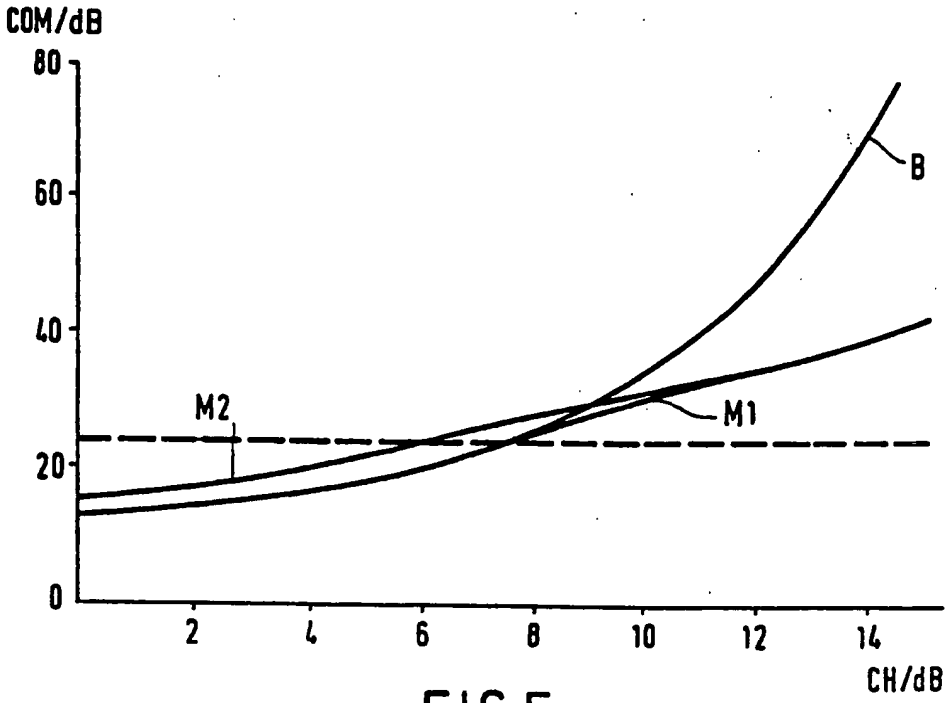

FIG.5

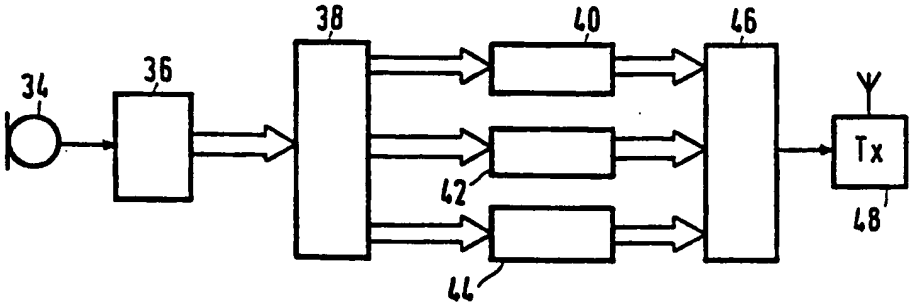

FIG.6

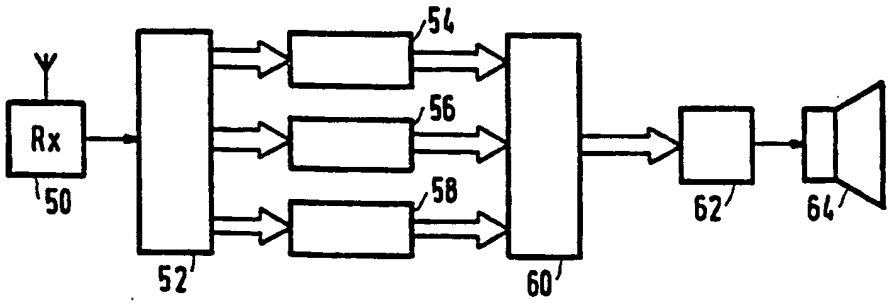

FIG.7

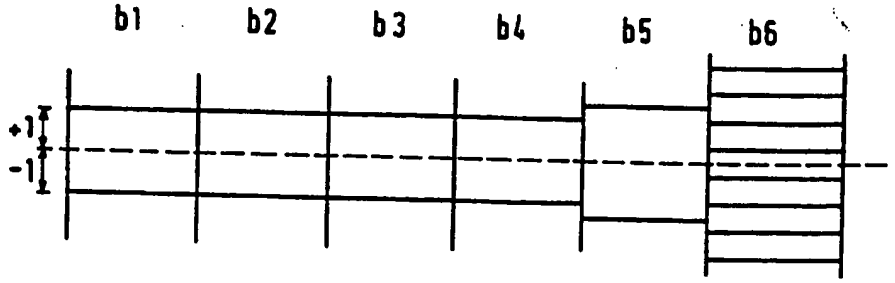

FIG.8

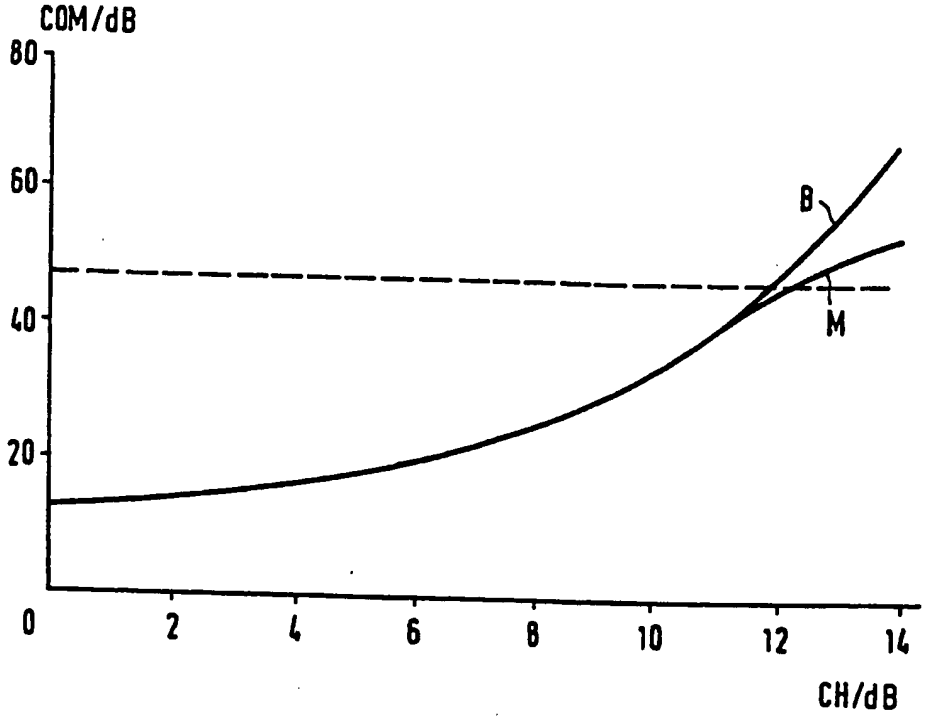

FIG.9

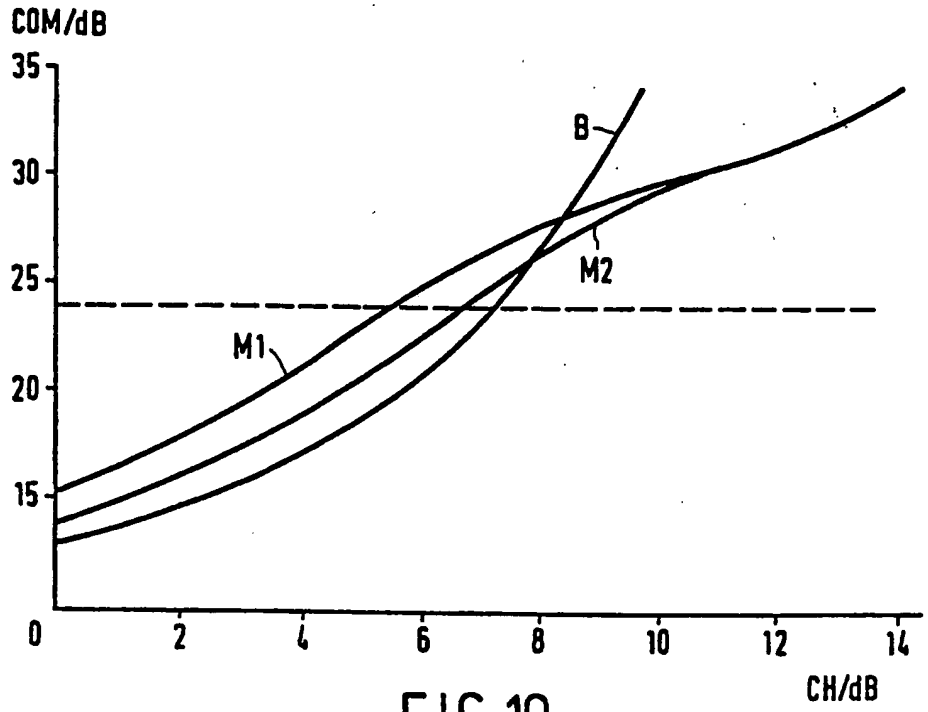
COM/dB
35
30
25
20
15
0
2
4
6
8
10
12
14
CH/dB
B
M2
M1

FIG.10

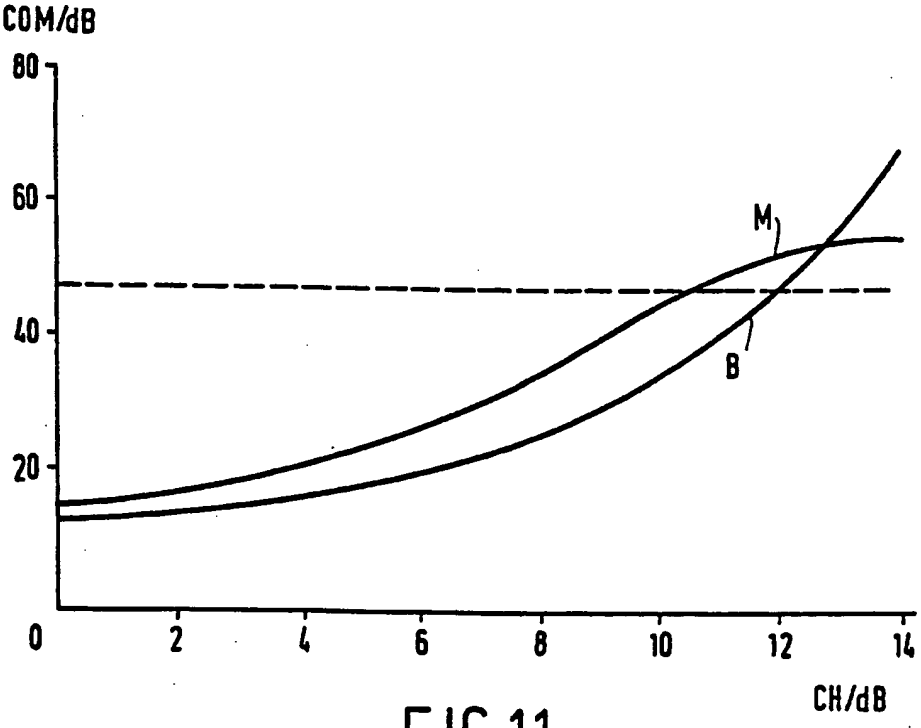
COM/dB
80
60
40
20
0
2
4
6
8
10
12
14
CH/dB
M
B

FIG.11